REMARKS

These amendments and remarks are being filed in response to the Office Action dated November 20, 2002. For the following reasons this application should be allowed, and the case passed to issue.

No new matter is introduced by this amendment. The amendment to claim 21 is supported by claim 1. New claim 23 is supported by claim 1; the specification at page 4, line 23 to page 5, line 23; and FIG. 1; which clearly disclose that the gate dielectric layer is located between the first electrode layer and the second electrode layer.

Claim Rejections Under 35 U.S.C. § 103

Claims 1-6, 8, 10, 21, and 22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Admitted Prior Art (APA) (Figure 7) in view of Tuan et al. (U.S. Pat. App. 2002/0151141) and Baliga (U.S. Pat. App. 2002/0177277). This rejection is traversed, and reconsideration and withdrawal thereof respectfully requested. The following is a comparison between the invention as claimed and the cited prior art.

An aspect of the invention, per claim 1, is a wafer comprising a base layer and an active layer formed on the base layer. A gate dielectric layer is formed on the active layer, a conductive layer is formed on the gate dielectric layer, and a plurality of isolation regions are formed in the wafer. The wafer is divided into a plurality of first portions, second portions, and third portions. The first portions comprise gate dielectric capacitors. The gate dielectric capacitors comprise a first electrode layer, an insulating layer, and a second electrode layer. The first electrode layer is formed from the active layer. The insulating layer is formed from the gate dielectric layer and the second electrode layer is formed from the conductive layer. The second portions comprise first dummy structures. The first

dummy structures comprise a first electrode layer and an insulating layer. The first electrode layer of the first dummy structures is formed from the active layer and the insulating layer of the first dummy structures is formed from the gate dielectric layer. The second portion does not contain the conductive layer. The third portions comprise second dummy structures, the second dummy structures comprise an insulating layer and a second electrode layer. The insulating layer of the second dummy structures is formed from an isolation region and the second electrode layer of the second dummy structures is formed from the conductive layer. The third portion does not contain the active layer.

In another aspect of the invention, per claim 21, the active layer comprises source/drain regions.

The Examiner asserted that Prior Art Figure 7 of the instant specification teaches a wafer comprising a base layer, gate dielectric layer, conductive layer, active region, a plurality of shallow isolation regions, and a metal interconnect. The Examiner acknowledged that the admitted prior art does not teach a wafer divided into a plurality of the claimed first, second, and third portions. The Examiner relied on Tuan et al. to provide a teaching of the third portion (second dummy structure) and Baliga to provide a teaching of the second portion (first dummy structure). The Examiner averred that the Tuan et al. dummy structures 141 correspond to the claimed second dummy structure and that the Baliga dummy structure 118c corresponds to the claimed first dummy structure. The Examiner concluded that it would have been obvious to modify the Admitted Prior Art gate structure to include the dummy structures of Tuan et al. and Baliga to provide a structure that can support high voltages.

The Admitted Prior art, Tuan et al., and Baliga, whether taken alone, or in combination, do not suggest the claimed wafer. The Examiner proposed combination does not disclose or suggest the claimed first portion or the first dummy structure. Baliga does not disclose the claimed first dummy structure as required by claims 1 and 21. In addition, contrary to the Examiner's assertion, reference no. 128 of Tuan et al. does not correspond to the claimed first electrode layer, as required by claim 21.

Claims 1 and 21 require that the second portion does not contain the conductive layer. The Examiner asserted that dummy structure 118c of Baliga comprises the first electrode layer and an insulating layer. As required by claims 1 and 21, the first electrode layer is formed from the active layer. Layer 118c of Baliga is formed from the same layer as 118a and 118b. However, layers 118a and 118b correspond to the conductive layer (second electrode layer) of a gate capacitor. The claimed active layer (first electrode layer) is a distinct layer from the conductive layer (second electrode layer). The conductive layer 118c of Baliga can not correspond to the claimed active layer because layer 118c is formed from the same layer as conductive layers 118a and 118b. Therefore, the combination of Baliga with Tuan et al. and the APA would not provide nor suggest the claimed wafer.

Claim 21 is further distinguishable because claim 21 requires that the active layer comprises source/drain regions. The Examiner asserted active layer 124 of Tuan et al. does not comprise source/drain regions.

Claims 1 and 21 are further distinguishable over the cited prior art because there is no suggestion in the cited references to combine them as asserted by the Examiner.

The dummy gate structures of Tuan et al. protect circuit elements during chemical-mechanical polishing (CMP). The APA does not disclose performing CMP after forming

circuit elements, as taught by Tuan et al. Therefore, there would be no suggestion to include the dummy structures of Tuan et al. in the wafer of the APA. Furthermore, Tuan et al. teach a high voltage portion 4402 of the semiconductor structure. Because the semiconductor structure of Tuan et al. already supports high voltage, there is no motivation to include the additional dummy structures of Baliga. One of ordinary skill in this art would not be motivated to include additional dummy structures to provide a structure that can support high voltages, when the structure already can support high voltages without the additional dummy structures.

Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge readily available to one of ordinary skill in the art. *In re Kotzab*, 217 F.3d 1365, 1370 55 USPQ2d 1313, 1317 (Fed. Cir. 2000); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992); *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). There is no suggestion in Tuan et al. or Baliga of substituting the claimed first and second dummy structures into the wafer of the Admitted Prior Art. There is no suggestion in Tuan et al. or Baliga of forming the claimed second portion in the wafer of the APA, as required by claims 1 and 21. There is no suggestion in Tuan et al. or Baliga to form the active layer comprising source/drain regions, as required by claim 21.

The mere fact that references can be modified does not render the resulting combination obvious unless the prior art also suggests the desirability of the modification. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). Tuan et al.

and Baliga do not suggest the desirability of forming the claimed first and second dummy structures and a gate dielectric capacitor.

The requisite motivation to support the ultimate legal conclusion of obviousness under 35 U.S.C. § 103 is not an abstract concept, but must stem from the applied prior art as a whole and realistically impel one having ordinary skill in the art to modify a specific reference in a specific manner to arrive at a specifically claimed invention. *In re Deuel*, 51 F.3d 1552, 34 USPQ2d 1210 (Fed. Cir. 1995); *In re Newell*, 891 F.2d 899, 13 USPQ2d 1248 (Fed. Cir. 1989). Accordingly, the Examiner is charged with the initial burden of identifying a source in the applied prior art for the requisite realistic motivation. *Smiths Industries Medical System v. Vital Signs, Inc.*, 183 F.3d 1347, 51 USPQ2d 1415 (Fed. Cir. 1999); *In re Mayne*, 104 F.3d 1339, 41 USPQ2d 1449 (Fed. Cir. 1997). There is no motivation in Tuan et al. or Baliga to form a wafer comprising the claimed first and second dummy structures and a gate dielectric capacitor.

The only teaching of the claimed wafer comprising a plurality of first portions, second portions comprising a first dummy structure, and third portions comprising a second dummy structure is found in Applicants' disclosure. However, the teaching or suggestion to make a claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicants' disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). The Examiner's conclusion of obviousness is not supported by any factual evidence. The Examiner has not provided a factual basis for asserting that the combination of the Admitted Prior Art, Tuan et al., and Baliga would provide the claimed invention. The Examiner's retrospective assessment of the claimed invention and use of unsupported conclusory statements are not legally sufficient to generate a case of

prima facie obviousness. The motivation for modifying the prior art must come from the prior art and must be based on facts.

The dependent claims further distinguish the claimed invention, for example, claim 4 further requires that the active layer comprises doped silicon. Claim 5 further requires an interconnect layer formed over the conductive layer. Claim 8 further requires a silicon electrode contacting an isolation region. Claim 10 further requires that the gate dielectric capacitor is a transistor. Claim 22 further requires that the silicon electrode is an electrically isolated polysilicon electrode that contacts an isolation region of the second dummy pattern. The cited prior art does not suggest the claimed wafer with these additional limitations.

New claim 23 is distinguishable over the cited prior art. The cited prior art does not suggest the claimed wafer wherein the gate dielectric layer is located between the first electrode layer and the second electrode layer, as required by claim 23.

In light of the Amendments and Remarks above, this application should be allowed and the case passed to issue. If there are any questions regarding this application, a telephone call to the undersigned would be appreciated to expedite the prosecution of the application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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